



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,081	08/23/2001	Charles Clark Jablonski	01-840	4215

24319 7590 12/07/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER

AMAYA, CARLOS DAVID

ART UNIT	PAPER NUMBER
----------	--------------

2836

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,081	JABLONSKI ET AL.	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2006.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 14 and 17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-7 is/are allowed.
- 6) ☒ Claim(s) 14 and 17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This communication is responsive to amendments received on 09/28/2006.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 14, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Alston (US 6,327,635).

With respect to claim 14 Alston discloses a method implemented by an interface circuit (the interface circuit is composed of the connection point of the add on card with bus 106) for supplying a computer logic circuit (add-on card 200) with first and second inputs having respective first and second predetermined voltage levels (Figure 2 shows power supply 202 providing two different voltages on lines 206 and 208 for the add-on card), that are different from each other and from ground (as shown in figure 3 the voltages on line 214 and 214 are different from each other and from ground), the method comprising: providing the computer logic circuit with the first input having the first predetermined voltage level based upon a first supply voltage (On Figure 2 the first supply voltage is supply to the add-on card 200 via line 214); determining if a second supply voltage that is different from the first supply voltage and from ground is present (Driver 302, Column 4 lines 35-37); and providing the computer logic circuit with the second input having the second predetermined voltage level (One of the voltages provided to the selection circuit is selected among the voltages provided), wherein

Art Unit: 2836

providing the second input comprises providing the second input having the second predetermined voltage level based upon both the first and second supply voltages if the second supply voltage is present (The voltages are tested and if both voltages are present the second (low voltage) is selected), and wherein providing the second input comprises providing the second input having the second predetermined voltage level based only upon the first supply voltage if the second supply voltage is unavailable (If only the second voltage is present than this voltage is selected having the second predetermined voltage).

With respect to claim 17 Alston discloses a method according to Claim 14 further comprising isolating the second supply voltage and the computer logic circuit by permitting the second supply voltage to be provided to the computer logic circuit without permitting the computer logic circuit to drive the second supply voltage (Figure 2 shows the computer logic circuit (add-on card 200) comprising of a power source selection circuit 210 comprising switches 310 and 312, this switches isolate the second supply voltage, thus it enables protection to the computer logic circuit, without letting the circuit drive the second power supply on line 212).

Allowable Subject Matter

3. Claims 1-7 are allowed.

Claim 1 is allowable over the prior art of record, because the prior art of record does not disclose "and interface circuit comprising a regulator for generating an output having the second predetermined voltage level in response to the first supply voltage; and a second power supply circuit for providing an output having the second

Art Unit: 2836

predetermined voltage level in response to a second supply voltage that is different from the first supply voltage and from ground, wherein said regulator and said second power supply circuit cooperate to provide the second input having the second predetermined voltage level in instances in which the second supply voltage is present”.

Response to Arguments

4. Applicant's arguments filed 09/28/2006 regarding claim 14 have been fully considered but they are not persuasive.

Alston discloses a computer logic circuit (add-on card 200) implemented by an interface circuit (connection between the bus 106 and add-on card) this card is provided with two different power supplies that are different from each other and ground as shown in figure 3. The card is composed of Power source selection circuit 210 as shown in Figure 3 the second supply and the regulator in cooperation with inverter 306 cooperate to supply the second predetermined voltage when the second supply is present.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

Art Unit: 2836

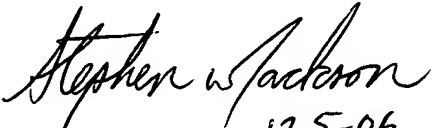
shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Amaya whose telephone number is (571) 272-8941. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CA


12-5-06

STEPHEN W. JACKSON
PRIMARY EXAMINER